REMARKS

Reconsideration of the application is requested.

Applicant acknowledges the Examiner's confirmation of receipt of applicant's After Final Amendment amending claims 1, 3, and 5 and the receipt for a Request for Continued Examination under 37 CFR 1.114 of the instant application.

Claims 1-6 are pending in the application and were rejected in the above-identified Office Action. Claims 1, 3, and 5 have been amended in this response.

More specifically, in item 4 on page 2 of the above-identified Office Action, claims 1, 2, 5, and 6 were rejected as being obvious over Applicant's Allegedly Admitted Prior Art (hereinafter **AAAPA**) in view of U.S. Patent No. 5,046,039 to *Ugajin, et al.* (hereinafter '**039**) under 35 U.S.C. § 103(a).

In item 5 on page 5 of the above-identified Office Action, claims 3 and 4 were rejected as being obvious over **AAAPA** in view of '**039** and further in view of U.S. Patent No. 5,673,416 to *Chee, et al.* (hereinafter '**416**) under 35 U.S.C. § 103(a).

The rejections have been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. No new matter is believed to have been added.

Support for the changes in claim 1 may be found in the specification in the paragraph bridging pages 3 and 4 and on pages 13-18 in combination with FIGS. 2-4 of the instant application.

Moreover, the amendments to claim 3 that pertain to the cooperation of the microprocessor 4 with the second data bus 7 are both shown in FIG. 1 and supported, in particular, in the second paragraph on page 5 and on pages 18-19 in combination with FIG. 5.

Claim 5 amendments are supported on pages 13 to 14 in combination with FIG. 2.

Before discussing the prior art in detail, it is believed that a brief review of the invention as currently claimed, would be helpful. More specifically, one element of the invention clarified and accentuated by the most recent amendments to claims 1, 3, and 5 is the adaptive adjustment of the memory size in use by the microprocessor 4 in both the

reception memory 1 and transmission memory 9. As will be explained in more detail below, FIG. 3 clearly indicates that before the first data transfer is completed from the HDLC reception Line to the microprocessor, a Stat signal is sent from the HDLC transmitter to the microprocessor. Moreover, the microprocessor sends a RFBS signal to the HDLC Receiver indicating "**a size of the memory for a following writing procedure in said memory**" before the first Ack signal is sent from the microprocessor to the HDLC Receiver. Neither the RFBS signal nor the early Stat signal is present in **AAAPA** (FIG 6A & 6B).

Specifically, amended Claim 1 calls for, *inter alia*, an improved ISDN-data transmission method for transmitting digital data divided up into HDLC **data frames of variable lengths** from a first data bus to a second data bus operated asynchronously with respect to the first data bus and controlled by a microprocessor. The method includes the steps of:

Writing **digital data of a given data frame** to a memory having **a settable size**;

informing the microprocessor, in a form of an **interrupt signal** generated by a memory control unit, **if** the memory is **full** or **if** the memory contains an entry indicating **an end of a respective data frame.**

setting via the microprocessor **a size** of the memory **for a following writing procedure in said memory**; and

transmitting from the microprocessor to the memory control unit an acknowledgment of a reception of **the data being read out from the memory**.

The amended claim 1 clarifies that the adaptive adjustment of the size of memory is important "**for a following writing procedure in said memory**" as recited in claim 1. Independent claims 3 and 5 contain similar language.

The **AAAPA** reference discloses an HDLC reception line, an HDLC receiver having a large FIFO receiver memory, a microprocessor, a HDLC transmitter having a FIFO transmission memory, and an HDLC transmission line. The HDLC receiver configuration in **AAAPA** only triggers an interrupt signal when the FIFO reception memory is full or if the received D-channel signals include a frame end.

As previously mentioned the length of the D-channel frame varies in both **AAAPA** and the instant application, but in **AAAPA** when the length is longer than the capacity of the FIFO reception memory the interrupt signal will not prompt the microprocessor to receive the data until the FIFO reception memory is full. Since the microprocessor in **AAAPA** will not even start making a response signal until after the microprocessor has read the data, the entire FIFO reception memory must be read before the response data can be written. This delay between reception and transmission in **AAAPA** is

sufficient to cause connection difficulties between subscribers.

In contrast, the present invention provides a microprocessor 4 that reads data from variable length data frames from a first data bus 5 and writes the data into a first memory 1. The microprocessor also writes the data in a second memory 9 so that the data can be delivered to a second data bus 7. The amount of data stored in the first memory 1 that will be read out by the microprocessor 4 upon receiving an interrupt is recorded in an RBC register. Subsequently, the microprocessor 4 writes a value that is to be available for the further data reception into an RFBS register. The RFBS register contains the amount of memory needed for the next writing procedure in the memory.

Initially, the memory size of the memory in the instant invention might be adaptively adjusted to be very small and increasingly adjusted by the microprocessor towards the maximum data frame size after receipt of a very long data frame. This configuration increases reliability and decreases connection difficulties, especially when compared with respect to the configuration disclosed in **AAAPA**.

Specifically, the present invention is able to transmit a confirming D-channel signal to a respective subscriber very early and very shortly after the initial receipt of a long data frame, see for example FIG. 3. But the overall number of interrupts is not necessarily increased, because the microprocessor, as a result of the adaptive adjustments through the RFBS register, is able, in the meantime, to increase the available memory space.

While it is clear that this adaptive adjustment process is applicable to the transmission portion of the configuration in FIG. 1 of the instant application, a similar adaptive adjustment cooperation exists between the microprocessor 4 and the second memory 9 and is explicitly described in claim 3 of the instant application.

A second memory control 8, which is associated with the second memory 9, indicates to the microprocessor 4 when the second memory 9 is ready to receive new data. Alternatively, the microprocessor 4 can determine the condition of the second memory 9 through its own query. Once the second memory is ready to receive new data, the microprocessor 4 writes data previously read out from the first memory 1 and adaptively adjusts the size of the second memory 9 for the subsequent writing process of data to a desired value. This

adjustment provides the present invention with an optimization of the size of the second memory 9 independent of the size of the data frame that is to be transmitted, another contrast to the constant memory size disclosed in **AAAPA**. In this manner the number of triggered interrupts can be minimized and the efficiency of the microprocessor increased relative to the configuration disclosed in **AAAPA**.

The **'039** reference discloses a buffer management system for a communication device. An intermediate storage is provided in **'039** between the transmitting device and receiving device. **'039 thereby pertains to variable partitioning of an intermediate memory between transmitting and receiving devices.** Any such buffering or partitioning is NOT the object of the instant application.

In contrast, the instant application provides an intermediate memory that can receive data frames of variable lengths or sizes and uses an adaptive adjustment of the memory size of the used memory. Exemplary memory devices include a FIFO memory where the memory can be dynamically adjusted between two reading processes of the microcontroller. As a result the microcontroller of the instant application can specifically and dynamically adjust the size of the intermediate memory that is to be read by the microcontroller

depending on what content the respective data frame has, which is just being written into the memory on the other side of the intermediate memory.

Moreover, in '039 the intermediate memory is designed to receive uniformly structured data, such as individual bytes or blocks of a constant size. For example, described system is easily configured to handle the constant block size of ATM, because the beginning and end of a data frame are predetermined and thus known. Because of this fact, the data structure information in '039 does not even need to consider adaptive adjustments due to the beginning and end of variable data frames as in the instant invention.

Clearly, **AAAPA** does not show "setting via the microprocessor a size of the memory **for a following writing procedure in said memory**" as recited in claims 1 and 3 of the instant application. Nor does **AAAPA** teach or suggest "a second register storing, **for a following writing procedure**, a present size of memory, said second register having a content selectively modifiable with each read cycle of the microprocessor" as recited in claim 5 of the instant application. Moreover, '039 does not overcome the deficiencies of **AAAPA**.

The '416 reference discloses memory request control unit for use in a DRAM interface. Although '416 does include a FIFO module, '416 not teach or suggest using HDLC data frames of variable lengths to transmit data from a first data bus to a second data bus operated asynchronously with respect to the first data bus. Perhaps more importantly, '416 does not overcome the previously discussed deficiencies of AAAPA and '039.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1, 3, or 5. Claims 1, 3, and 5 are, therefore, believed to be patentable over the art. The dependent claims 2, 4, and 6 are believed to be patentable as well because they all are ultimately dependent on claims 1, 3, and 5 respectively.

In view of the foregoing, reconsideration and allowance of claims 1-6 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

Petition for extension is herewith made. The extension fee for response within a period of one month pursuant to Section 1.136(a) in the amount of $110.00 in accordance with Section 1.17 is enclosed herewith. If an additional extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicant

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